

Appln No. 10/784,114
Amdt date July 26, 2005
Reply to Office Action of April 26, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Previously presented) A convolutional interleaving system comprising:

a memory array having a plurality of array cells, M, with selected array cells storing symbols therein, the memory array having a memory block length, N and an interleave depth, D;

a write commutator operably connected with the memory array for writing a symbol to a preselected memory cell at a first time; and

a read commutator operably connected with the memory array for reading the written symbol from the preselected memory cell at a second time, wherein a difference between the second time and the first time is a predetermined delay, the predetermined delay being related to a desired structure of the memory array,

wherein the memory array includes a plurality of interleaver array rows, the plurality of interleaver array rows including a selected row, R_i , having a row length, S, determined by:

$$S = \left\lfloor \frac{(D-1)}{N} R_i \right\rfloor + 1,$$

wherein i is the number of the row,

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wherein M is determined by:

$$M = \frac{(N-1)D + \gcd(N, D-1) + 1}{2}, \text{ and}$$

wherein $\gcd(N, D) = 1$.

3. (Previously presented) The convolutional interleaving system of Claim 2, wherein one of the read commutator and the write commutator changes position using a predetermined modulo technique.

4. (Previously presented) The convolutional interleaving system of Claim 3, wherein the predetermined modulo technique comprises incrementing the position of the one of the read commutator and the write commutator by K rows, wherein $K > 1$.

5. (Previously presented) The convolutional interleaving system of Claim 3, wherein the predetermined modulo technique comprises incrementing the position of the one of the read commutator and the write commutator by K rows, wherein K satisfies:

$$KD \bmod N \equiv 1;$$

6. (Previously presented) The convolutional interleaving system of Claim 2, wherein one of the read commutator and the write commutator changes position using a predetermined modulo technique, the predetermined modulo technique incrementing the

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position of the one of the read commutator and the write commutator by K rows, wherein $K > 1$ and K satisfies:

$$KD \bmod N = 1.$$

7. (Previously presented) The convolutional interleaving system of Claim 6, wherein the predetermined modulo technique comprises incrementing the position of the other of the read commutator and the write commutator by one cell.

8. (Previously presented) The convolutional interleaving system of Claim 2, further comprising a row position pointer for selecting a memory cell within a selected one of the plural array rows.

9. (Previously Presented) The convolutional interleaving system of Claim 2, wherein the memory array further includes a plurality of deinterleaver array rows, the plurality of deinterleaver array rows including a selected row, R_d , having a row length, U, determined by:

$$U = \left\lfloor \frac{(D-1)}{N} (N-1-R_d) \right\rfloor + 1,$$

wherein d is the number of the row.

10. (Previously presented) The convolutional interleaving system of Claim 2, wherein the predetermined delay is selectable among:

a. $(D - 1) (i \bmod N)$ symbols, wherein $\gcd(N, D) = 1$;

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- b. $(N) (i \bmod D)$ symbols, wherein $D|N$;
- c. $(D - 1) ((N-i-1) \bmod N)$ symbols, wherein $\gcd(N,D) = 1$;
and
- d. $(N) ((D-i-1) \bmod D)$ symbols, wherein $D|N$.

11. (Previously presented) The convolutional interleaving system of Claim 2, wherein the commutator position of one of the read commutator and the write commutator increments prior to a read operation.

12. (Previously presented) The convolutional interleaving system of Claim 2, wherein the commutator position of one of the read commutator and the write commutator increments after a write operation.

13. (Previously presented) The convolutional interleaving system of Claim 2, wherein one of the read commutator and the write commutator changes position using a predetermined finite difference equation technique.

14. - 21. (Canceled)